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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,856	08/07/2001	Craig Edward Hampel	RB1-037USC1	3540

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EXAMINER
PHAN, TRONG Q

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/924,856	Applicant(s) HAMPEL ET AL.	
	Examiner TRONG PHAN	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) *1-7,27,28,33,37 and 38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-17,19-26,29-32,34-36 and 39-47* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *29 January 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Drawings

1. The corrected Fig. 15 received on 1/29/03 has been accepted.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 8-11, 13-14 and 39-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawagoe, 5,680,354, in view of Yasuhiro, 5,730,830.

Kawagoe, 5,680,354, discloses in Fig. 1 an apparatus comprising:

a first XOR circuit Ex having: a first input to receive a first data in a first format at terminal 6, **a second input to receive an output signal S2 from defective bit address registering circuit 4, which is seen to be periodically toggling between "H" level and "L" level as shown in Figs. 3 and 5,** other than the first data, and an output to provide the first data in a second format through inverter 8 and a first buffer; for writing data to the memory device 1 as recited in claim 39;

a second XOR circuit ExO having a first input coupled to the output of the first XOR circuit Ex at node I/O; a second input to receive the periodic signal S2 other than the first data; and an output to provide the first data in the first format to terminal 6;

output circuit 7 being obviously considered as a second buffer as recited in claim 14;

an address buffer (not shown) for providing address buffer output signal A0...An, /A0.../An (see line 36-37, column 2).

What is not shown in Fig. 1 of Kawagoe, 5,680,354, is the burst counter as recited in claim 11.

Yashuhiro, 5,703,830, discloses in Fig. 3 Prior Art the teaching of using column address buffer & burst counter 1 for incrementing odd address signal YADD1 such as A3, A5 ... by +2 in response to clock cycles C3, C5... as shown in Fig. 4B Prior Art and for incrementing even address signal YADD2 such as A4, A6 ... by +2 in response to clock cycles C4, C6... as shown in Fig. 4D Prior Art (see lines 57-63, column 3) which can be used in synchronous DRAM device.

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to utilize the column address buffer & burst counter 8 in Figs. 3, 4B and 4D Prior Art of Yashuhiro, 5,703,830, for the address buffer (not shown) in Fig. 1 of Kawagoe, 5,680,354, for generating the address signals

4. Claims 15-17 and 19-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al., 5,295,188, in view of Sumida et al., 4,071,889.

Wilson et al., 5,295,188, discloses in Fig. 3 a system comprising:

a first circuit 56 having a plurality of output terminals each being connected to each first input of each of a first plurality of XOR gates 74;

memory 60, having a number of memory locations as matrix T (see lines 40-42, column 13) and the noise bits above and to the right of the diagonal submatrices in the matrix T (see lines 3-4, column 13) which are pseudorandom numbers (see claims 10 and 22) such as recited in claim 36, and **including AND logic gate 64 providing an output signal, which is periodically toggling between the "one" logic level and the "zero"**

logic level (see lines 1-9, column 14), to the second inputs of first plurality of XOR gates 74;

a second circuit comprising buffer memory circuit 78 (see line 18, column 14) having a plurality of input terminals connected to the outputs of the first XOR gates 74;

a second plurality of XOR gates 84 each having a first input being coupled to the second circuit buffer memory circuit 78 and a second input being coupled to **the output signal from AND logic gate 64, which is periodically toggling between the "one" logic level and the "zero" logic level (see lines 1-9, column 14)**.

What is not shown in Fig. 3 Wilson et al., 5,295,188, is the shift register as recited in claims 16-17 and 19-20.

Sumida et al., 4,071,889, discloses in Fig. 7 a circuit having a shift register 512 acting as a buffer memory (see lines 11-13, column 12).

It would have been obvious under 35 USC 130(a) to one of the ordinary skill in the art at the time of the invention was made to utilize the shift register 512 in Fig. 7 of Sumida et al., 4,071,889, for the purpose of reading data.

Allowable Subject Matter

5. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG PHAN whose telephone number is (703) 308-4870. The examiner can normally be reached on M-F (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-4021 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Phan Trong

TRONG PHAN
PRIMARY EXAMINER

February 24, 2003